WHAT WE CLAIM ARE:

1. A compound semiconductor device comprising:

a substrate;

a channel layer disposed above said substrate and consisting essentially of GaN;

an electron supply layer disposed above said channel layer and consisting essentially of n-type $Al_qGa_{1-q}N$ ($0 < q \leq 1$);

a cap layer disposed above said electron supply layer and consisting essentially of n-type GaN;

a gate electrode disposed on said cap layer and forming a Schottky contact;

recesses formed on both sides of said gate electrode on source and drain sides by removing at least part of said cap layer, said recess having a bottom surface of a roughness larger than a roughness of a surface of said cap layer under said gate electrode;

a source electrode disposed on the bottom surface of said recess on the source side; and

a drain electrode disposed on the bottom surface of said recess on the drain side.

2. The compound semiconductor device according to claim 1, wherein the roughness of the surfaces of the recesses on the source and drain sides is in a range from about 1.5 times to about 10 times the roughness of the surface of said cap layer under said gate electrode.

3. The compound semiconductor device according to claim 1, further comprising a passivation film made of insulating material and covering said cap layer and said recesses on the source and drain sides.

4. The compound semiconductor device according to claim 3, wherein a notch is formed in at least said cap layer between said gate electrode and said drain electrode, and said passivation film covers a surface of said notch.

5. The compound semiconductor device according to claim 1, wherein another notch is formed in at least said cap layer between said gate electrode and said source electrode, and said passivation film covers a surface of said another notch.

6. The compound semiconductor device according to claim 5, wherein at least one of said notch and said another notch traverses said cap layer in a depth direction and reaches an inside of said electron supply layer.

7. The compound semiconductor device according to claim 1, wherein an electron affinity ß of said cap layer is larger than an electron affinity α of said electron supply layer, $ß > α$.

8. The compound semiconductor device according to claim 1, wherein at least one of said recesses on the source and drain sides reaches an interface between said cap layer and said electron supply layer, and the surface roughness makes said cap layer partially left and said electron supply layer partially exposed.

9. The compound semiconductor device according to claim 1, wherein said channel layer, said electron supply layer and said cap layer do not contain In.

10. The compound semiconductor device according to claim 1, wherein said recess on the source side is deeper than said recess on the drain side.

11. A method of manufacturing a compound semiconductor device comprising the steps of:

(a) epitaxially laminating above a substrate a channel layer consisting essentially of GaN, an electron supply layer consisting essentially of n-type $Al_qGa_{1-q}N$ ($0 < q \leq 1$) and a cap layer consisting essentially of n-type GaN, in this order recited;

(b) forming a gate electrode on said cap layer, said gate electrode having a Schottky contact;

(c) etching at least part of the cap layer to form recesses on both sides of said gate electrode on source and drain sides, in such a manner that a bottom surfaces of said recesses have a roughness larger than a roughness of a surface of said cap layer under said gate electrode; and

(d) forming a source electrode and a drain electrode on the bottom surfaces of said recesses on the source and drain sides.

12. The method of manufacturing a compound semiconductor device according to claim 11, wherein said step (c) partially leaves said cap layer and partially exposes said electron supply layer by positively utilizing said roughness, and said step (d) forms one or both of said source and drain electrodes so as to make one

or both contact both said cap layer and said electron supply layer.

13. The method of manufacturing a compound semiconductor device according to claim 11, further comprising a step of exposing the surfaces of said recesses to plasma after said step (c).

14. The method of manufacturing a compound semiconductor device according to claim 11, wherein said step (c) includes etching said recess on the source side by using a mask and etching said recess on the drain side by using another mask.

15. The method of manufacturing a compound semiconductor device according to claim 11, further comprising a step of forming a notch through said cap layer, said notch traversing in a depth direction said cap layer at least between said gate electrode and said drain electrode or between said source electrode and said gate electrode.